

Virtual Boy Technical Symposium

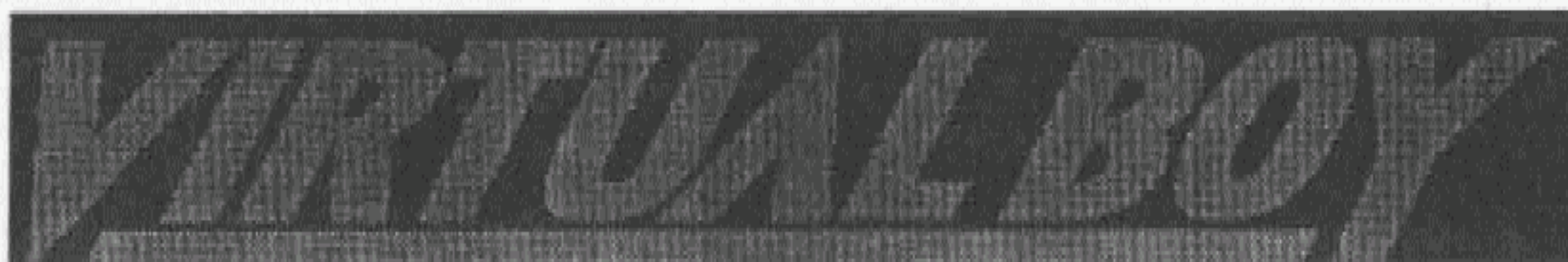


Bit Mapped Graphics
Virtual Sound Unit (VSU)
Serial Port, Controller Access



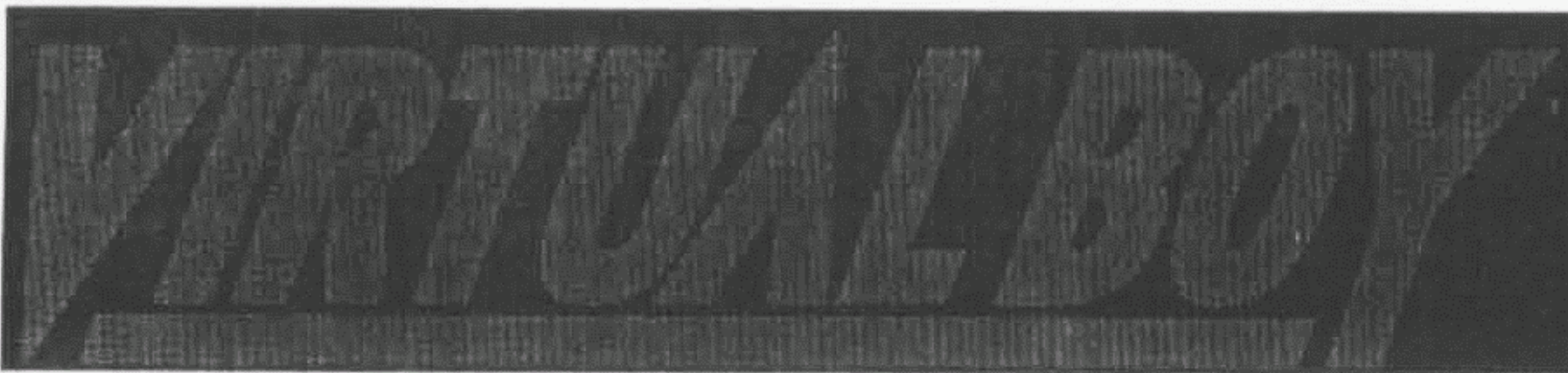
PLANET VIRTUAL BOY

[HTTP://WWW.VR32.DE](http://www.vr32.de)



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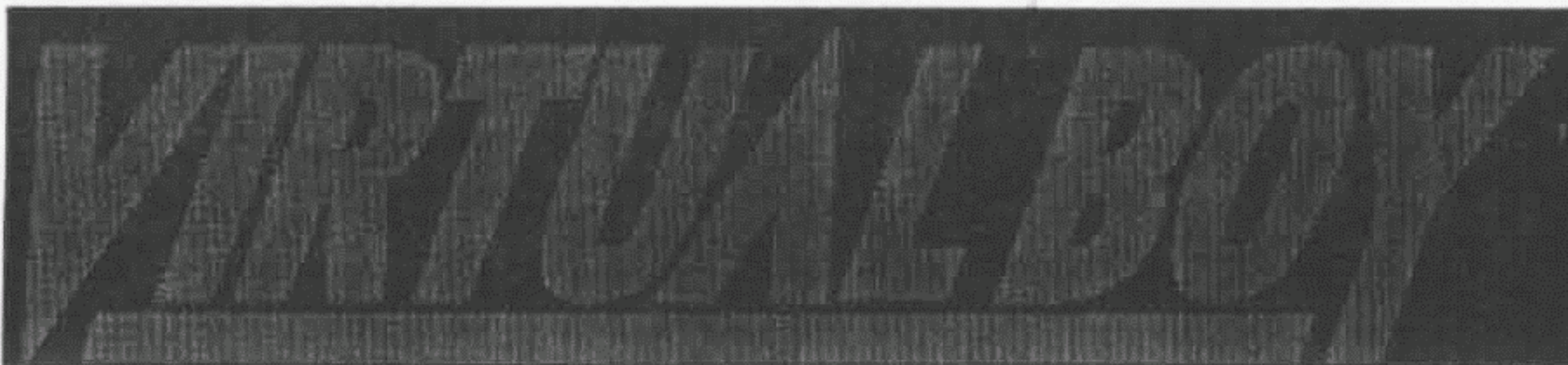
Bit Mapped Graphics



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VIP Frame Buffers

- Frame Buffers (FB)
 - ◆ Double Buffered Bit Mapped GFX
 - ◆ Useful for polygon and vector graphics
 - ◆ V810 Blt functions useful for quickly updating bitmaps
 - ◆ Can be combined with OBJ & BG graphics



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Bit Map Reality

- Bit Map Size
 - ◆ 384 (horizontal) x 224 (vertical) x 2 bits
 - ◆ Each eye has its own double Frame Buffers (FB)
 - ◆ Aspect ration of 1.71



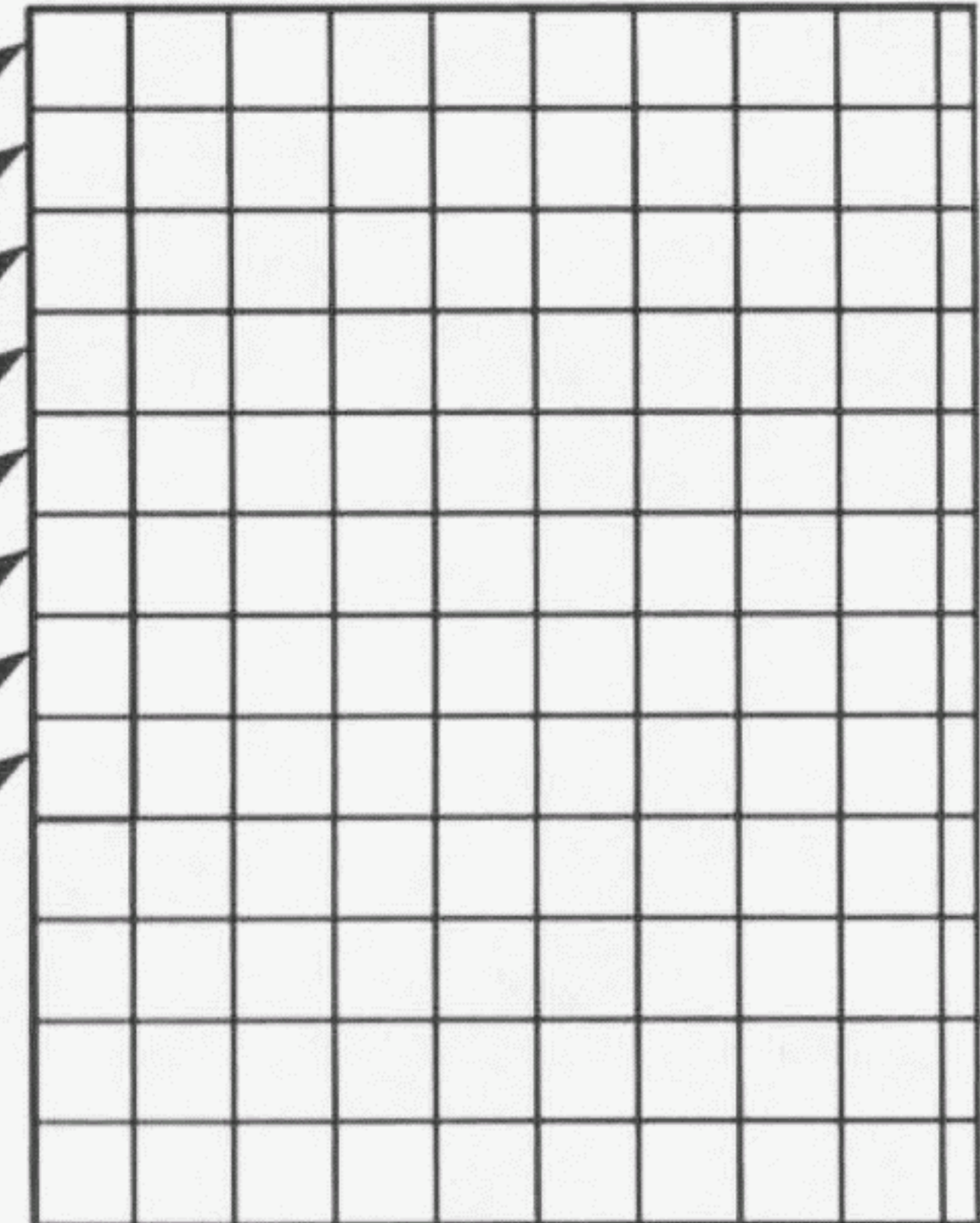
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Frame Buffer Configuration

2 Bytes = 8 pixels
2 Bits / Pixel.

Pixels arranged in columns,
Top -> Bottom, Left -> Right

Bit 0,1 of Address 0
Bit 2,3 of Address 0
Bit 4,5 of Address 0
Bit 6,7 of Address 0
Bit 0,1 of Address 1
Bit 2,3 of Address 1
Bit 4,5 of Address 1
Bit 6,7 of Address 1

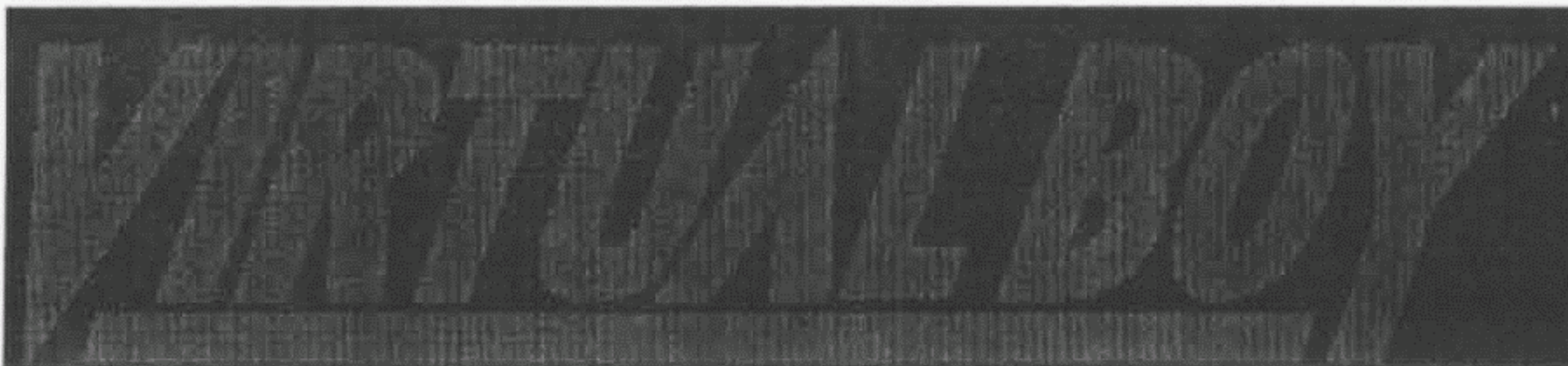


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Frame Buffer Memory Map

- 24 k bytes 4 buffers

FB 0	L_FB0	Left Screen Frame Buffer 0	0000 0000H~0000 5FFFFH
	R_FB0	Right Screen Frame Buffer 0	0001 0000H~0001 5FFFFH
FB 1	L_FB1	Left Screen Frame Buffer 1	0000 8000H~0000 DFFFFH
	R_FB1	Rigth Screen Frame Buffer 1	0001 8000H~0001 DFFFFH



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Using Frame Buffer Graphics

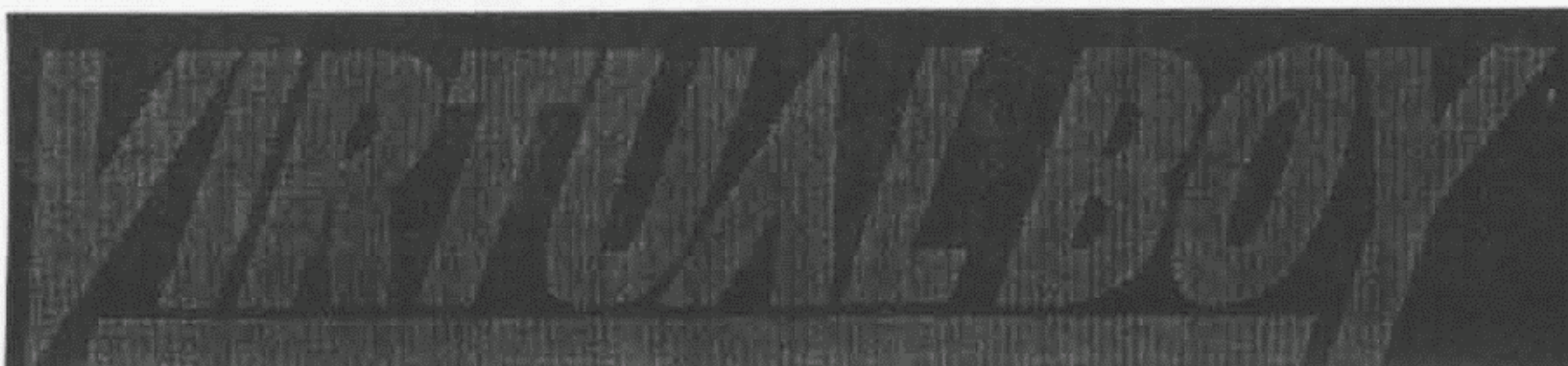
- Two registers control access to the VIP and its Frame Buffers.
 - ◆ Display Control Register
 - Provides display status.
 - Controls display status.



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Using Frame Buffer Graphics

- Two registers control access to the VIP and its Frame Buffers.
 - ◆ Drawing Control Register
 - Provides Drawing status.
 - Controls Drawing processes.



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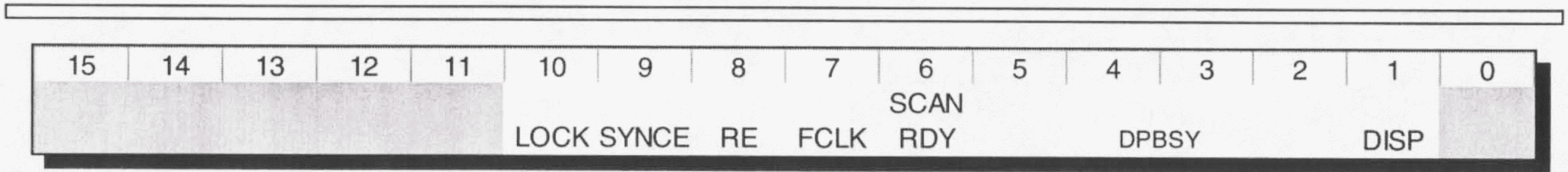
Display Control Register

- The VIP controls the FB display with read register, DPSTTS and write register, DPCTRL.
 - ◆ Turns display on/off.
 - ◆ Indicates display status
 - ◆ Indicates Frame Buffer currently being displayed



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Display Control Registers



- DISPLAY CONTROL READ REGISTER (DPSTTS)



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Display Control Registers

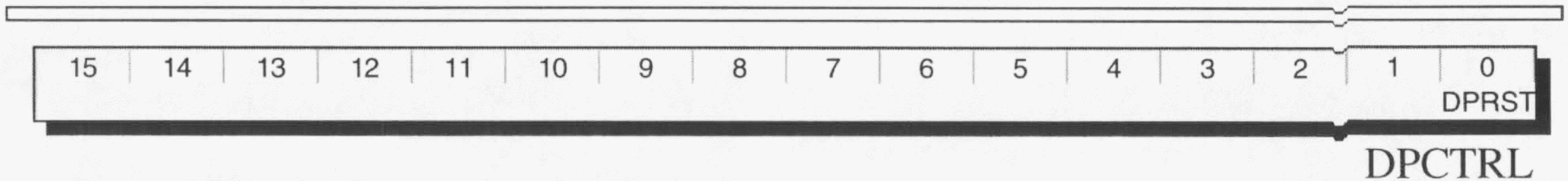
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK SYNCE RE								DISP DPRST							

- DISPLAY CONTROL WRITE REGISTER
(DPCTRL)



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Display Control Registers



- Flag description

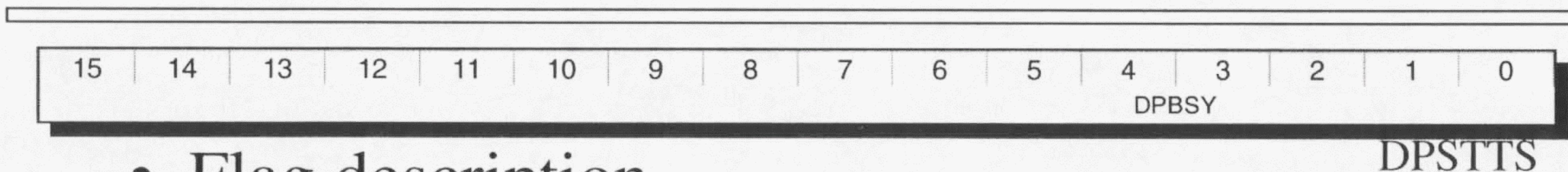
- ◆ DPRST

- 1: Reset VIP internal counter and mask VIP related IRQ's. Used to reset the VIP manually.
 - 0: no effect



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Display Control Registers



- Flag description

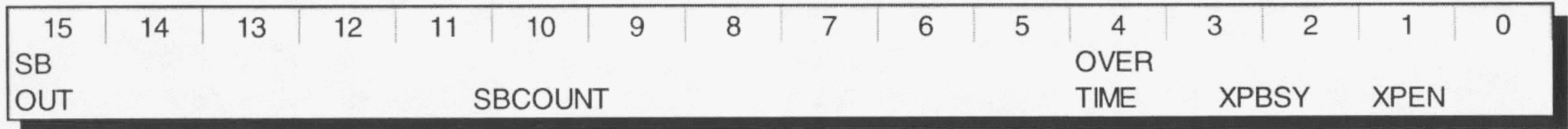
- ◆ DPBSY

- 0000b: Idle
- 0001b: Left-eye FB0 being displayed
- 0010b: Right-eye FB0 being displayed
- 0100b: Left-eye FB1 being displayed
- 1000b: Right-eye FB1 being displayed



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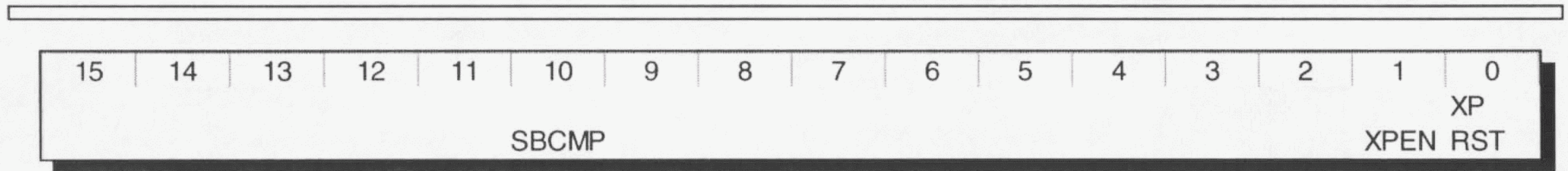
Drawing Control Registers



- DRAWING CONTROL READ REGISTER (XPSTTS)



Drawing Control Registers

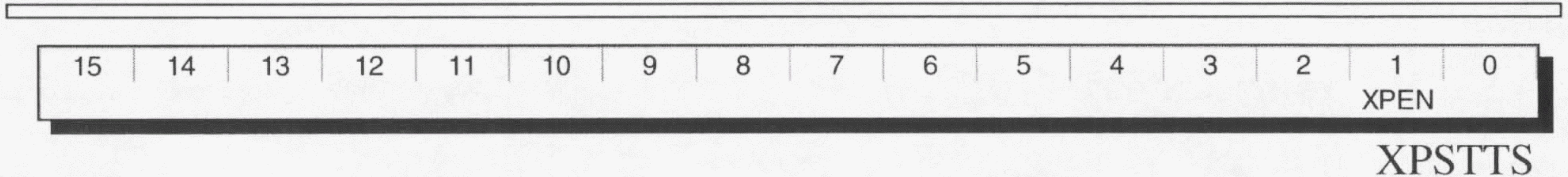


- DRAWING CONTROL WRITE REGISTER (XPCTRL)



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Drawing Control Registers

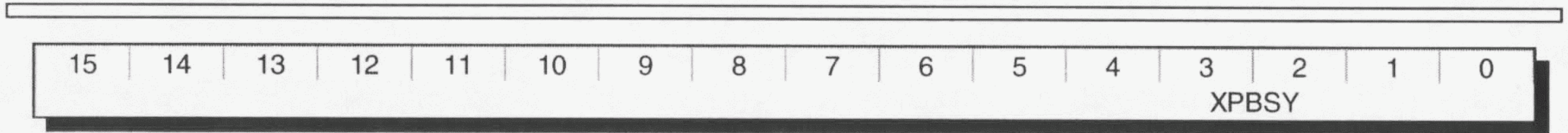


- Flag Descriptions
 - ◆ XPEN
 - ◆ This flag authorizes drawing to start at the beginning of the Game Frame



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Drawing Control Registers



- Flag Descriptions

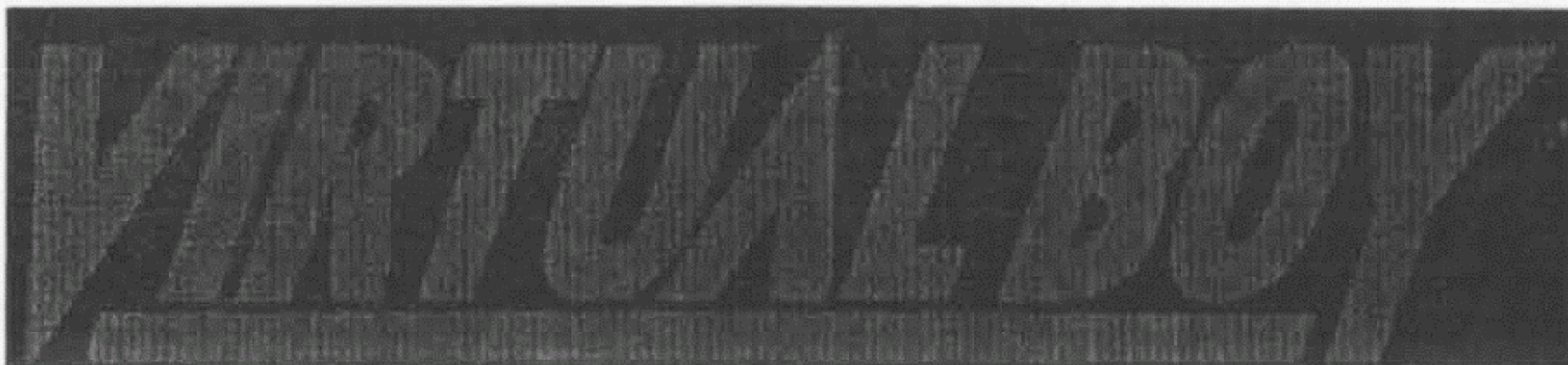
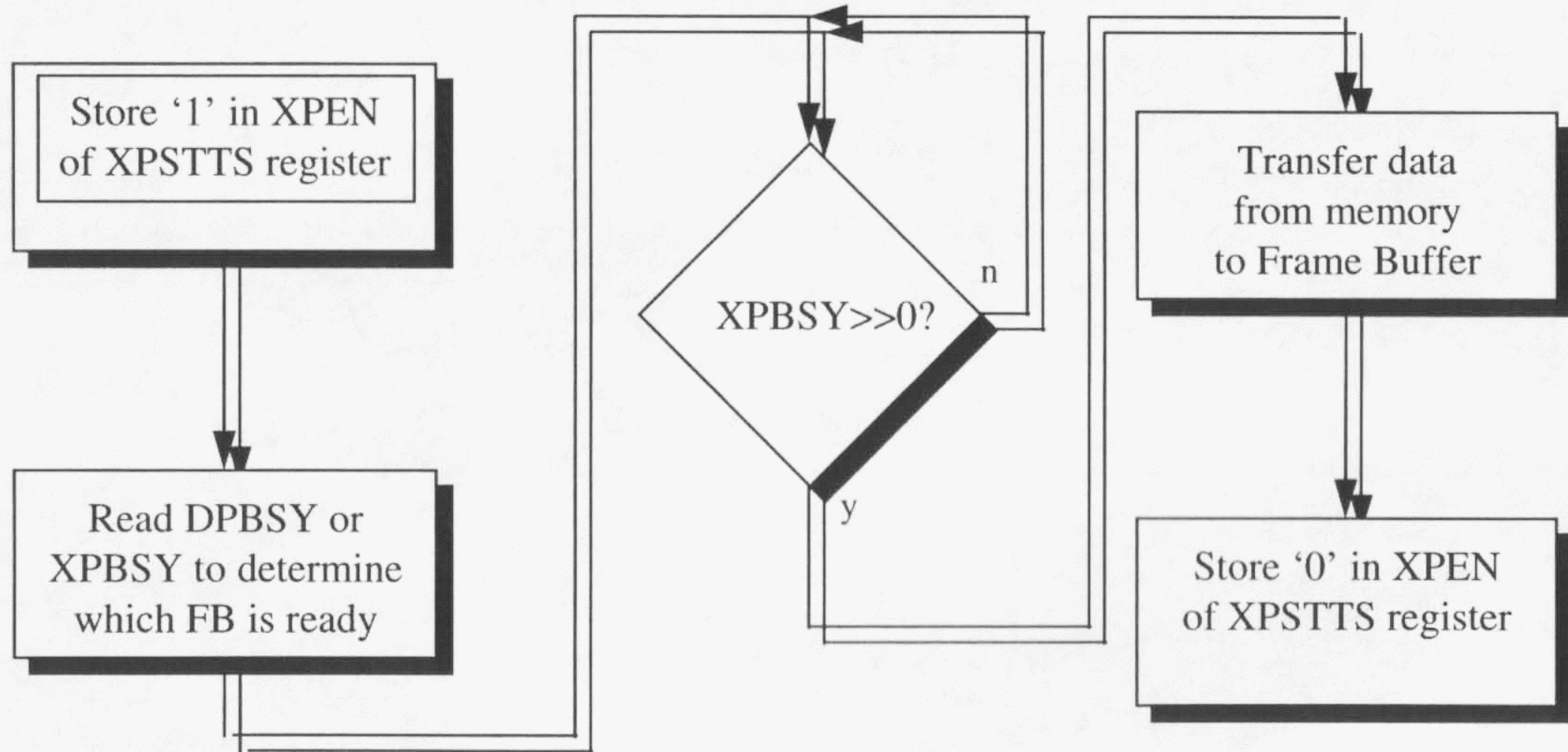
- ◆ XPBSY

- Indicates the status of drawing and screen processing.
 - 00b: idle
 - 01b: Screen editing FB0
 - 10b: Screen editing FB1



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Frame Buffer Drawing Process



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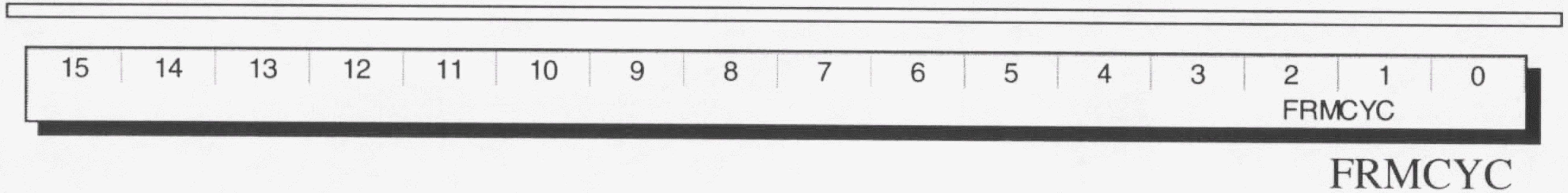
Important programming issues:

- Manual implementation of Parallax
 - ◆ Use caution not to violate programming cautions when creating bit-mapped images with graphics tools.
- Screen Size:
 - ◆ Each Column contains 64 bytes (256 vertical dots) only 56 bytes (224 vertical dots) are displayed



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Game Frame Control Register



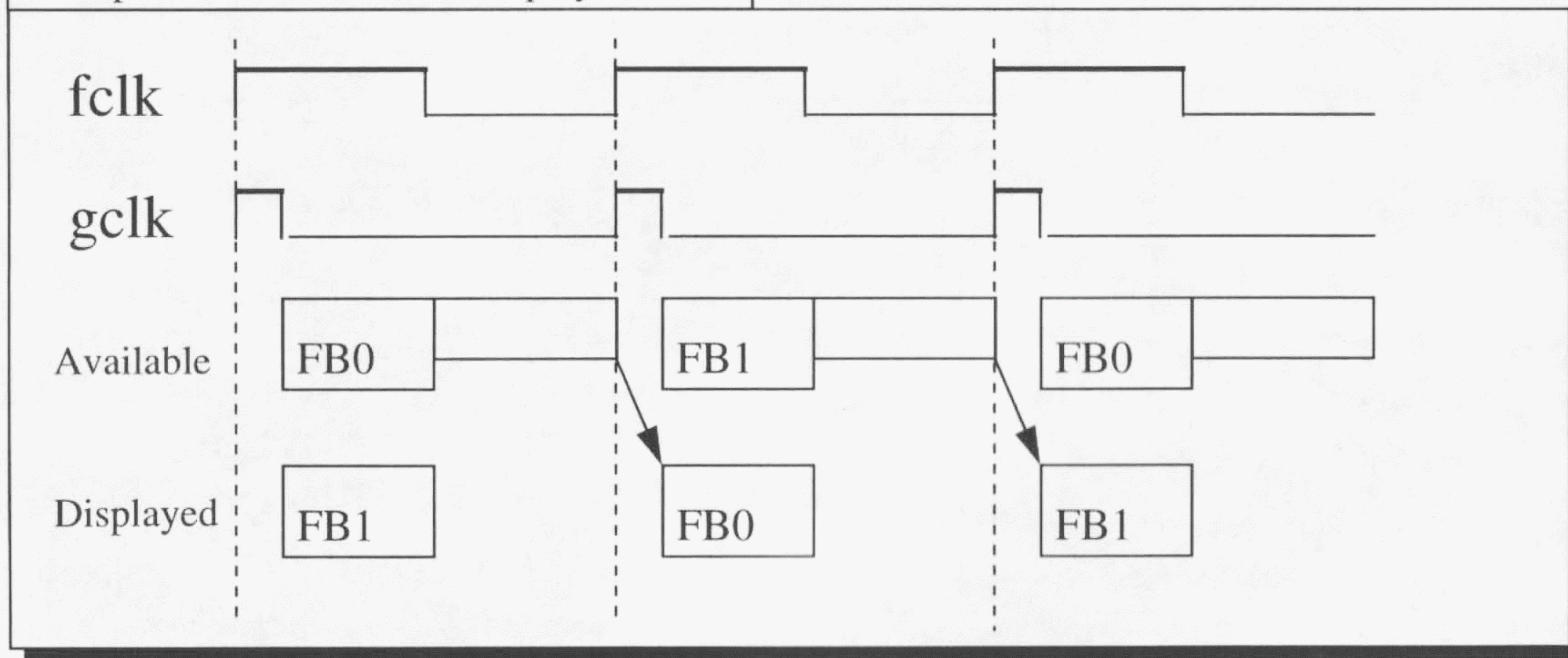
- FRMCYC values (1~16) Generates IRQ at the beginning of a GAME FRAME
 - ◆ Provides Frame Update Timing
 - ◆ Generates IRQ



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Game Frame Control

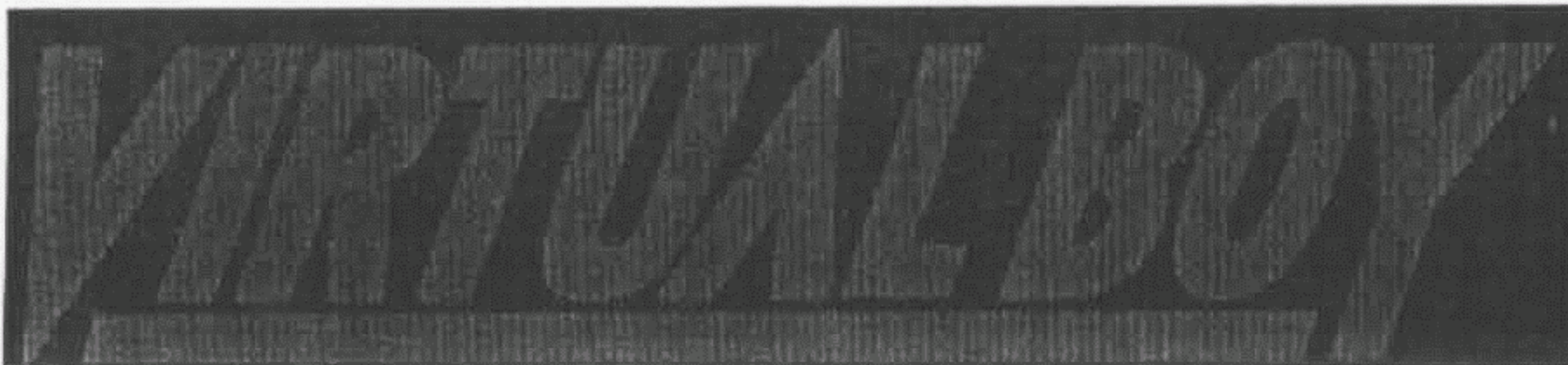
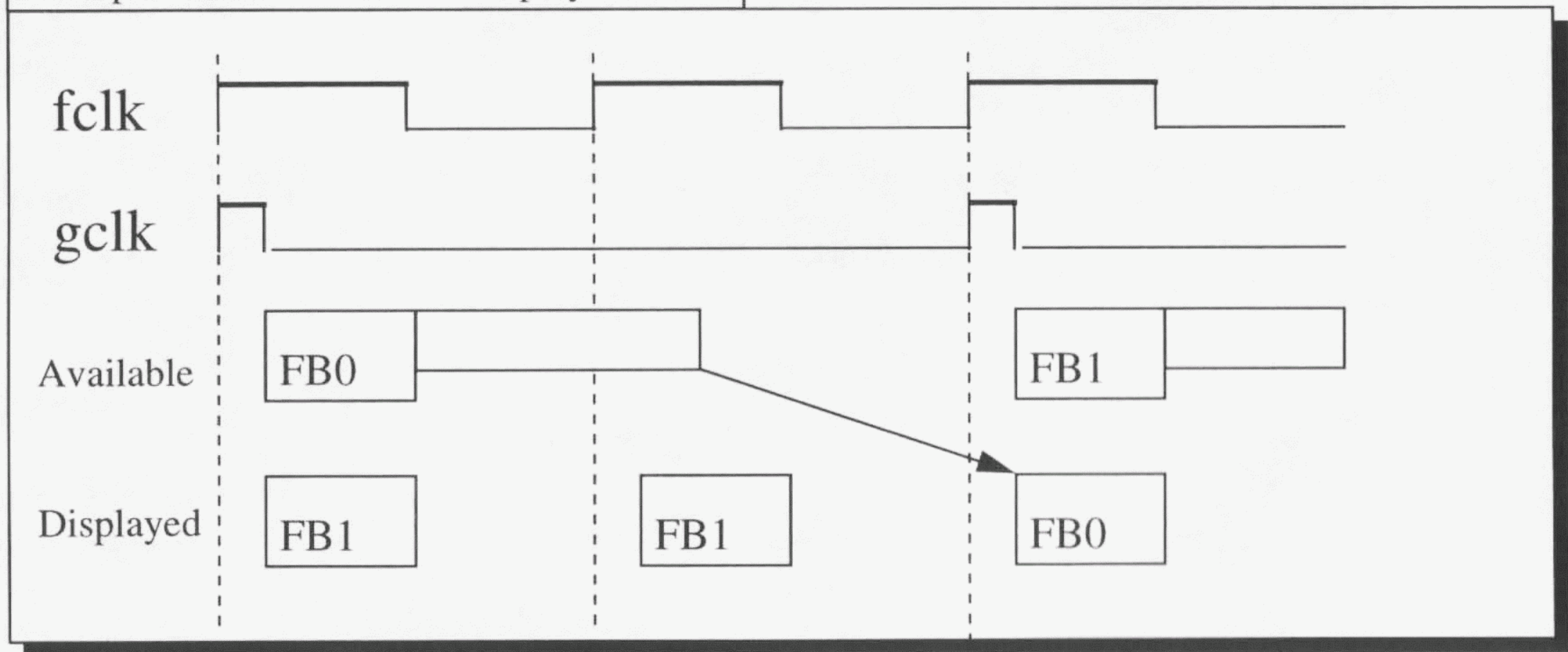
Example: Game Frame = 1 Display Frame



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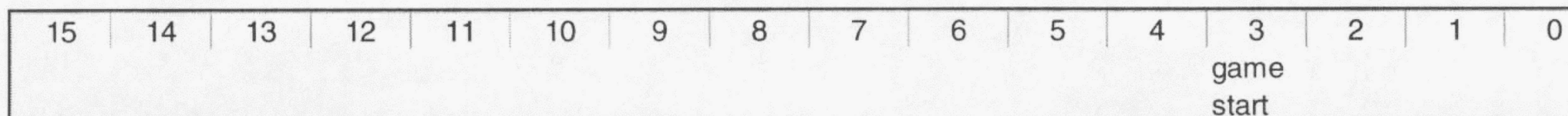
Game Frame Control

Example: Game Frame = 2 Display Frame

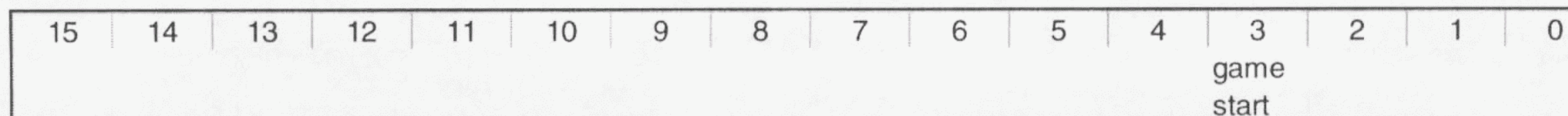


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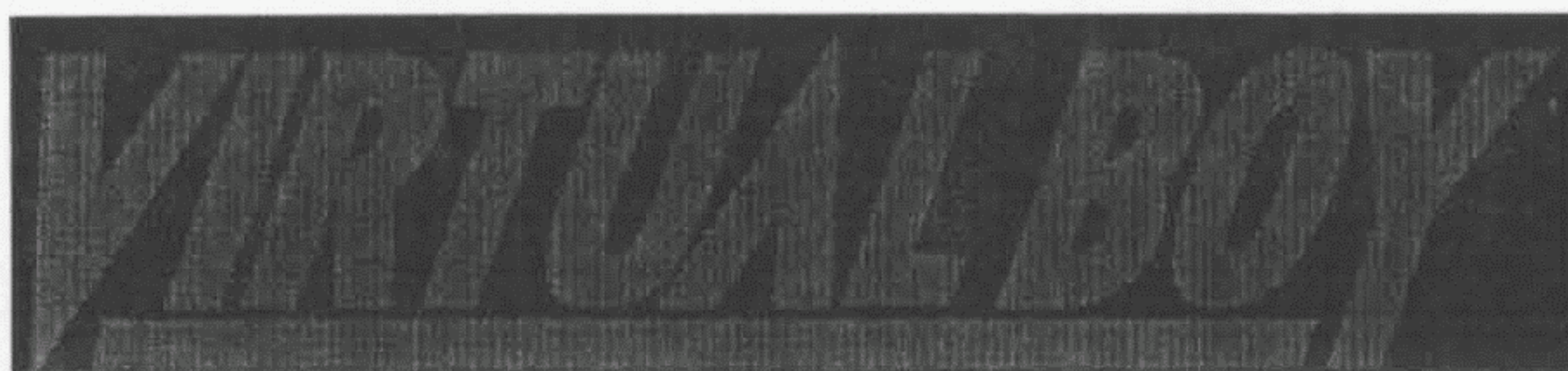
Game Frame Control IRQ



INTENB (interrupt enable)

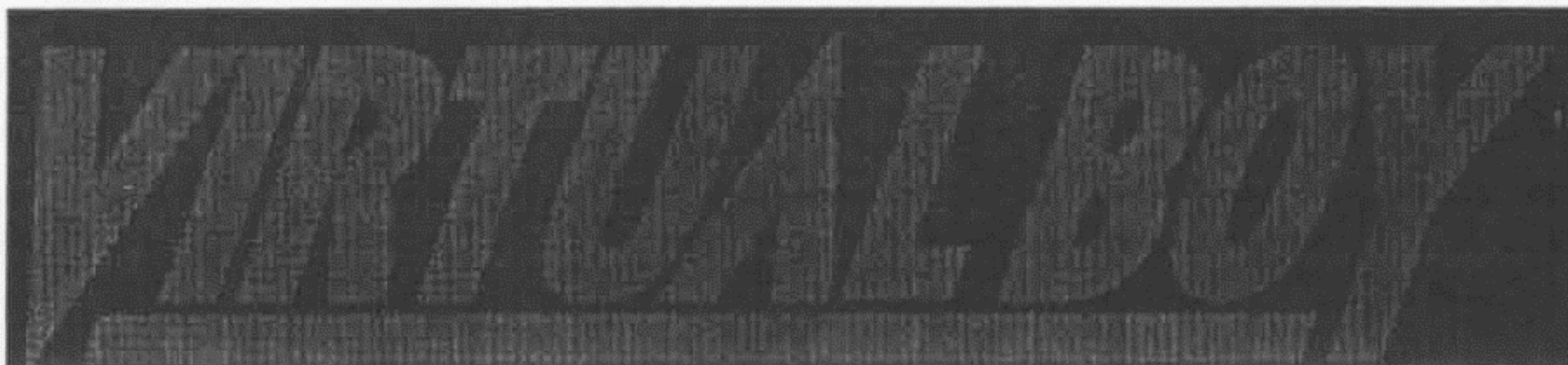
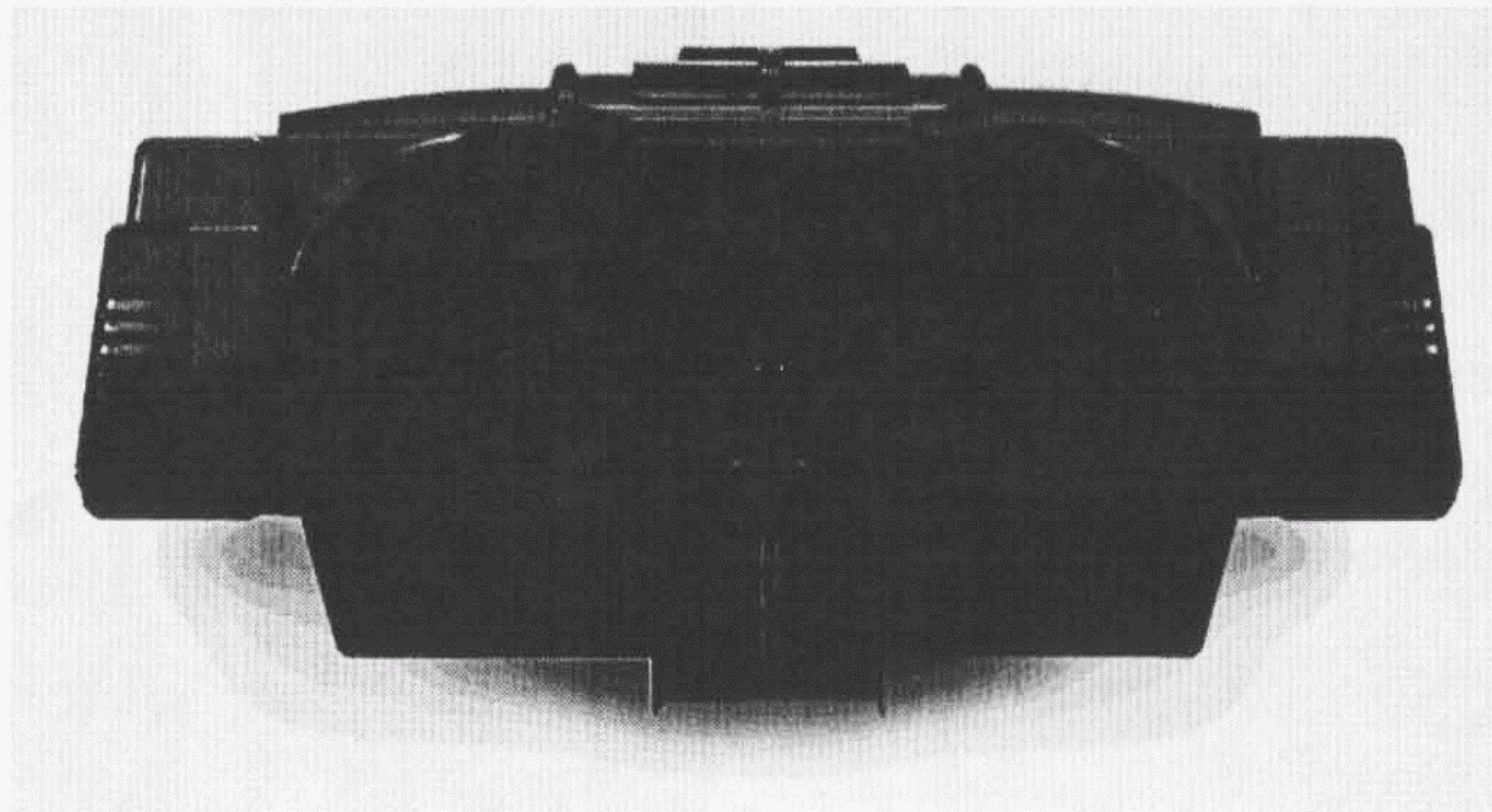


INTCLR (interrupt clear)



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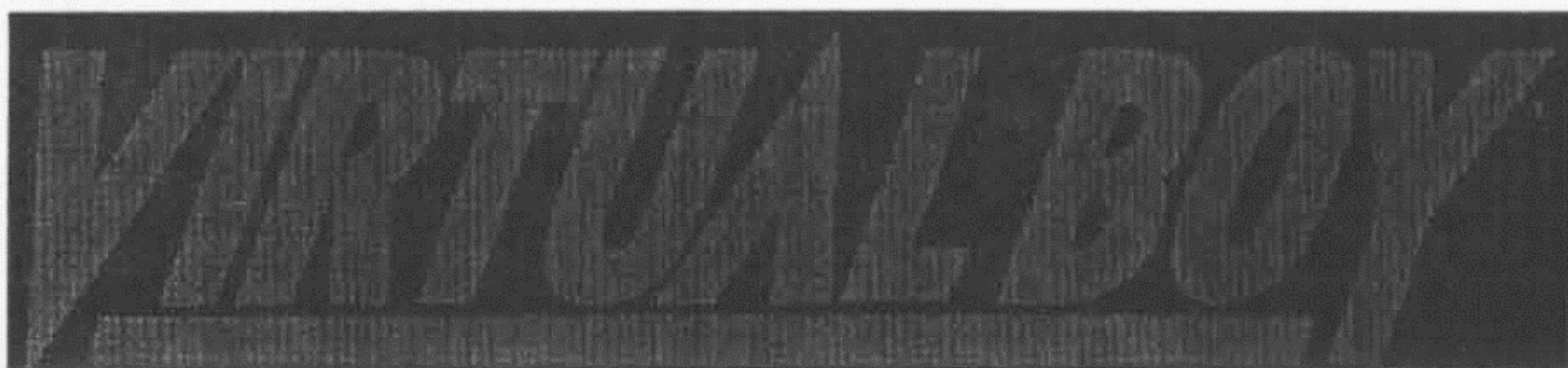
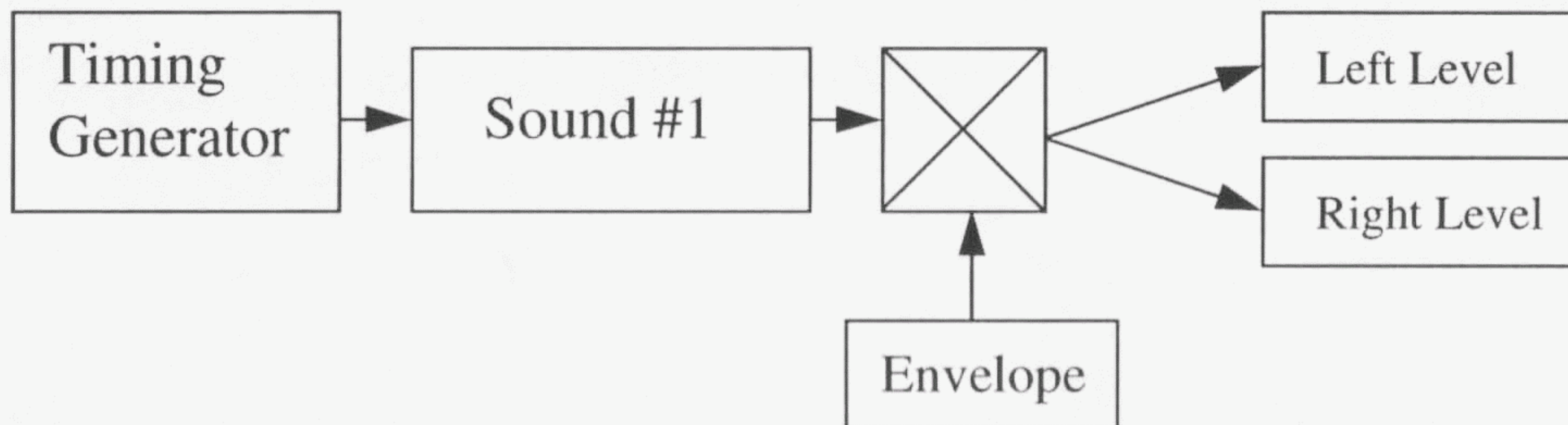
Virtual Sound Unit (VSU)



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Virtual Boy Audio

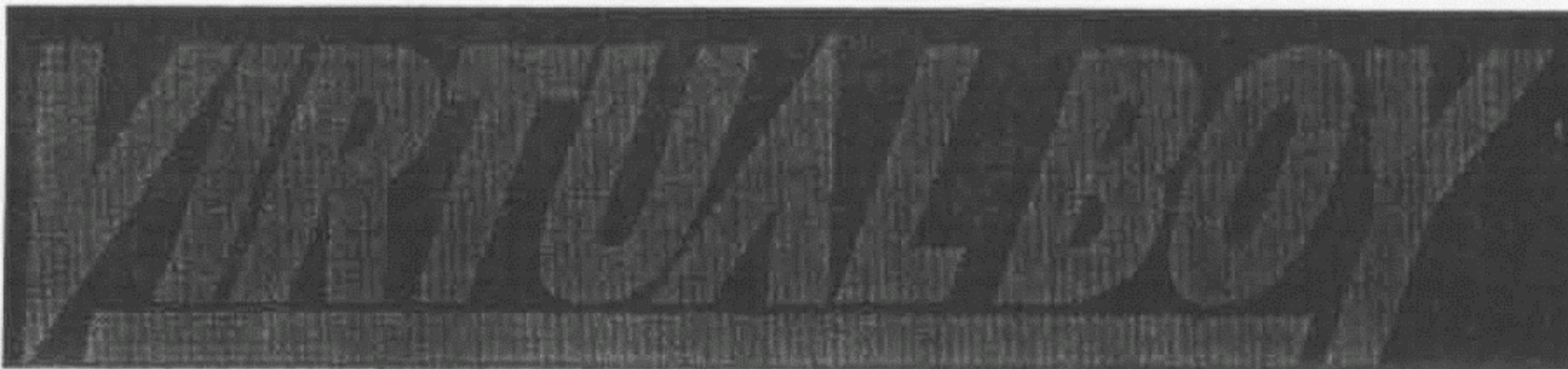
- Virtual Boy Sound Processor (VSU)



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VSU Functions

- Timing Generator
 - ◆ Divides 20 MHz clock to 5.00 MHz
 - ◆ 11 bit counter used to generate PITCH
 - ◆ SxFQH & SxFQL (high byte, Low byte)
 - ◆ $f = 5.00 \text{ MHz} / ((2048 - n) * 32) = \text{PITCH}$
 - $n = 0 \sim 2040$



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VSU Functions

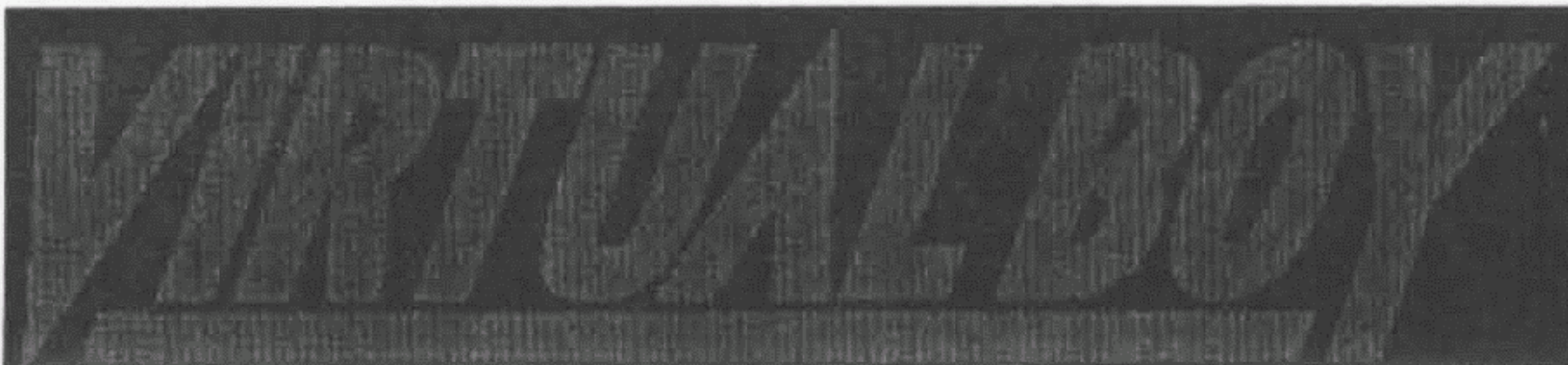
- Sound Data
 - ◆ Each Voice (except noise) consists of 6 bits x 32 words x 5 channels.
 - ◆ Sample rate is 41.7 KHz
 - ◆ 5 banks of “Waveform” data are provided
 - Allows quick change of voices
 - Simple audio “morphing”



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VSU Functions

- Envelope Generator
 - ◆ Uses delta Volume/Time technique
 - Set initial volume (0000b ~ 1111b)
 - Set increase / decrease flag
 - Set Envelope Step Time (15.4ms ~ 122.9ms)
 - Set once / repeat flag



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VSU Functions

- Panning
 - ◆ Main volume and sound locations are controlled with the Sound Output Level setting for the Left and Right channels
 - ◆ See table in your manual



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VSU Special Sounds

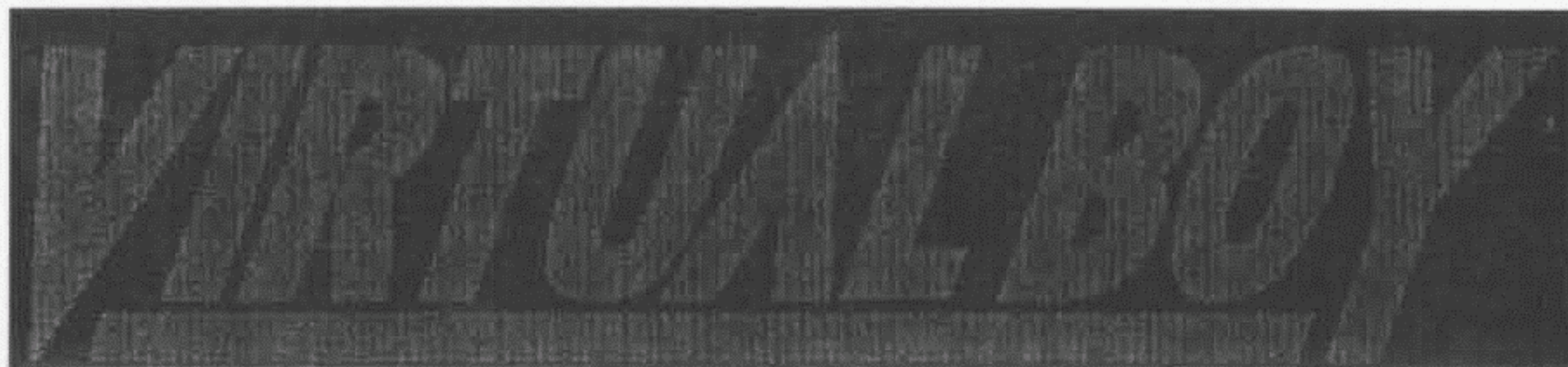
- Channel 5 (Sweep or Modulation)
 - ◆ RAM contains 32 bytes (8 bit signed) of modulation data
 - ◆ Modulation can be repeated or executed once
 - ◆ SWEEP functions shifts data right until value exceeds 7FFh



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VSU Special Functions

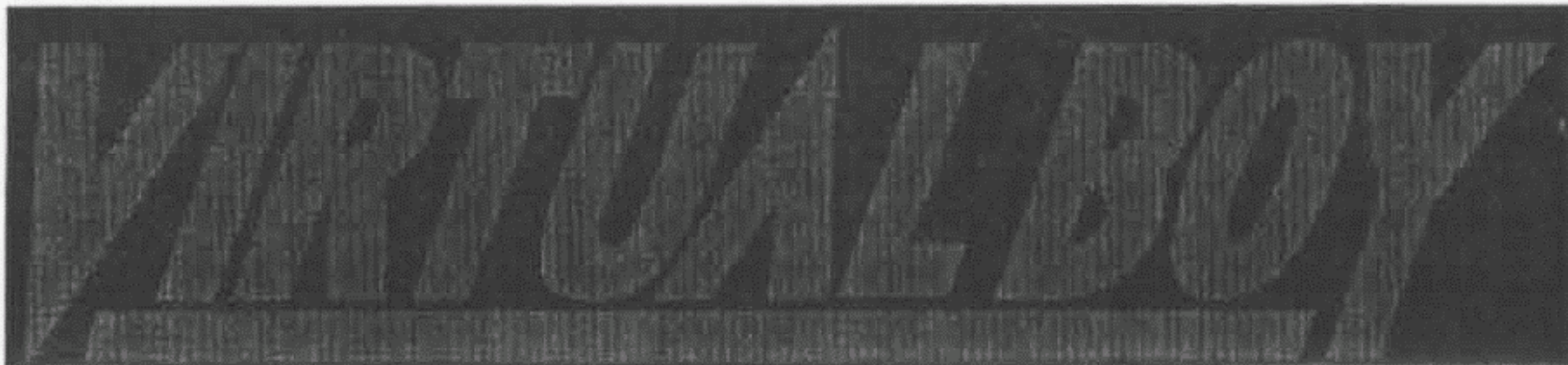
- Channel 6 (Noise)
 - ◆ M- type random number generator
 - ◆ 15 level shift register



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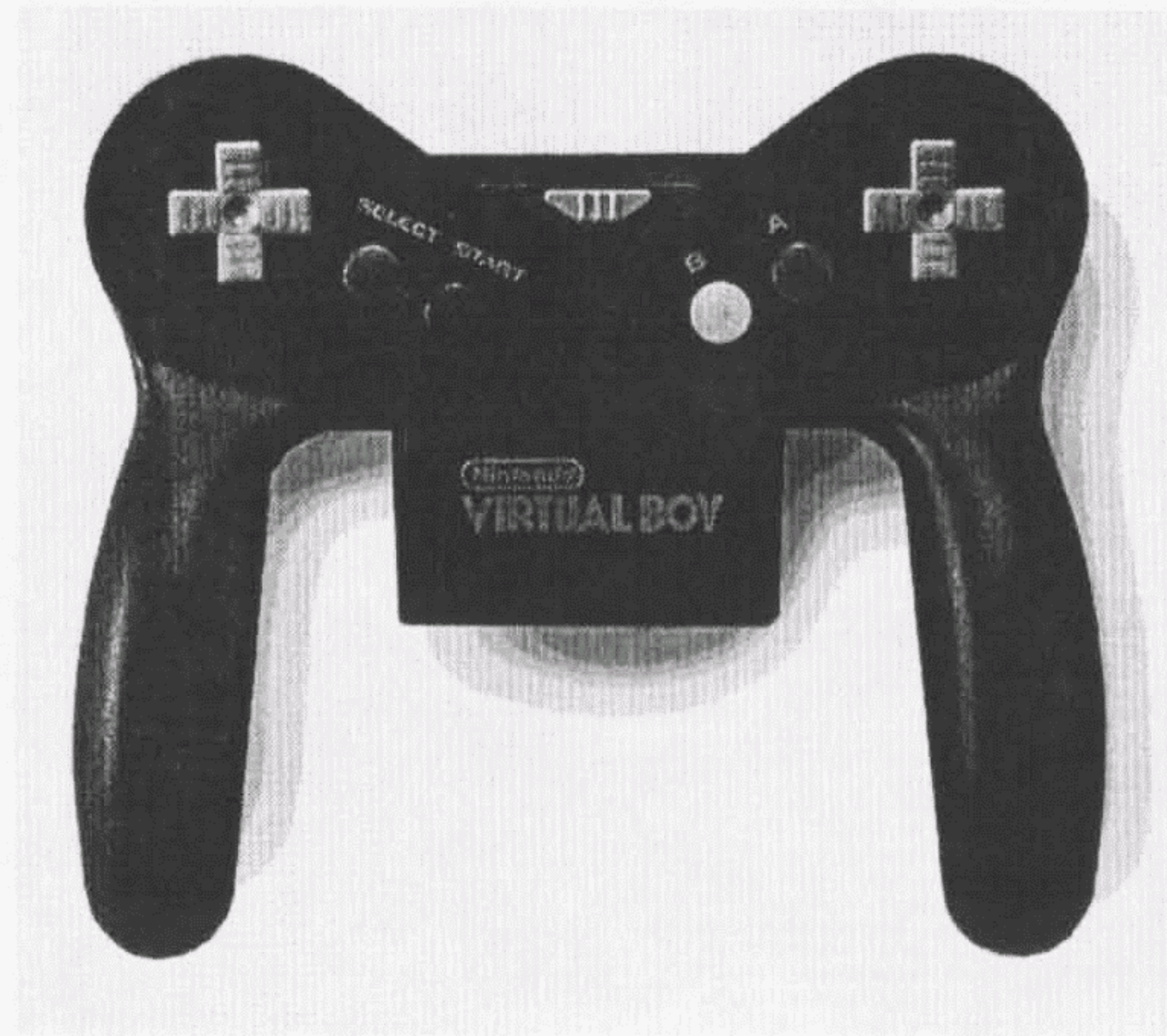
VSU Cautions

- Bits D4~D6 in the S5EV1 register for sound 5 are assigned to the sweep / modulations setting
- Bits D4~D6 in the S6EV1 register for SOUND 6 are assigned to M-type tap selection



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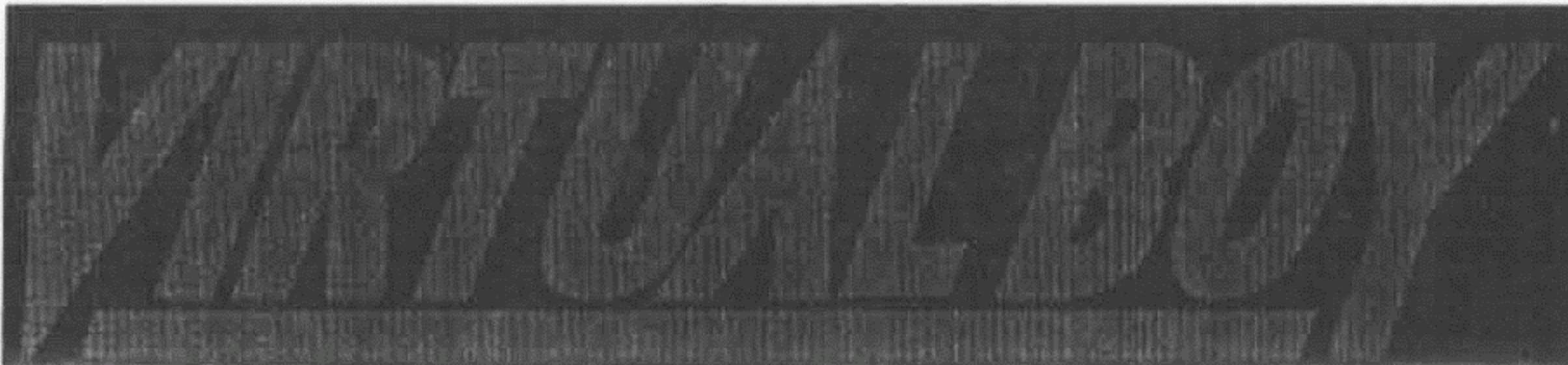
Serial Port, Controller Access



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Serial Port

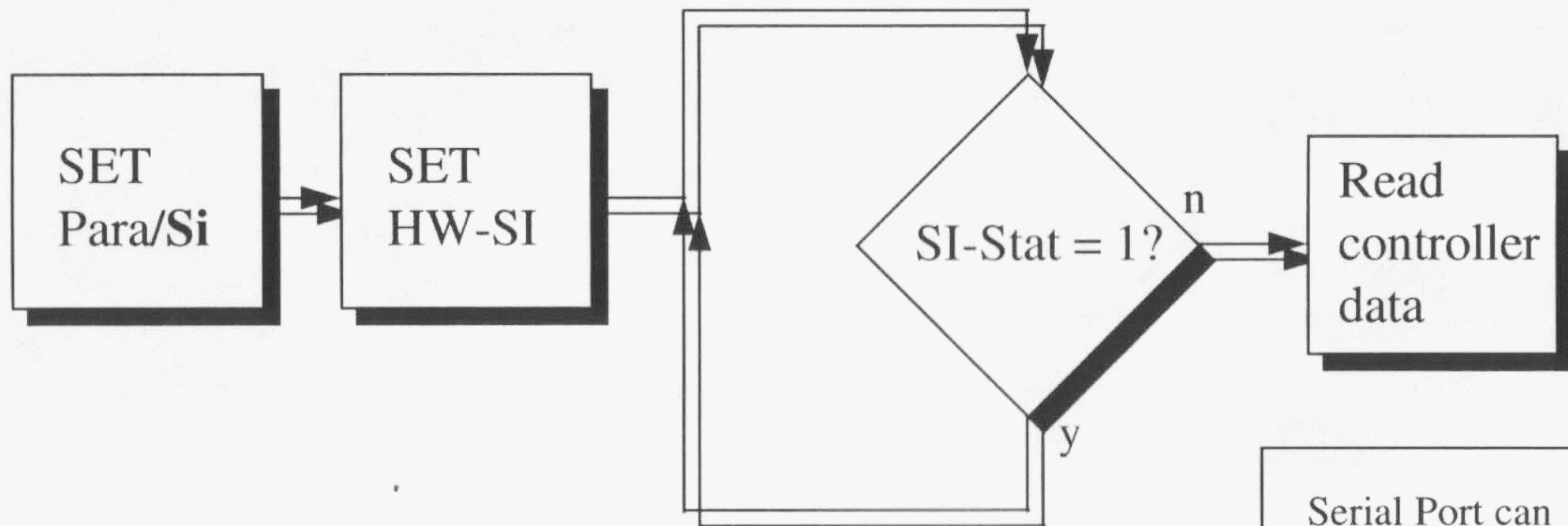
- Game Controller Communications
 - ◆ Serial interface to the VB Game Controller
 - ◆ 31.25 KHz clock speed
 - ◆ Data includes key data (key pressed), Controller ID and battery low indicator



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Controller Interface

- Software Interface (read controller w/software)

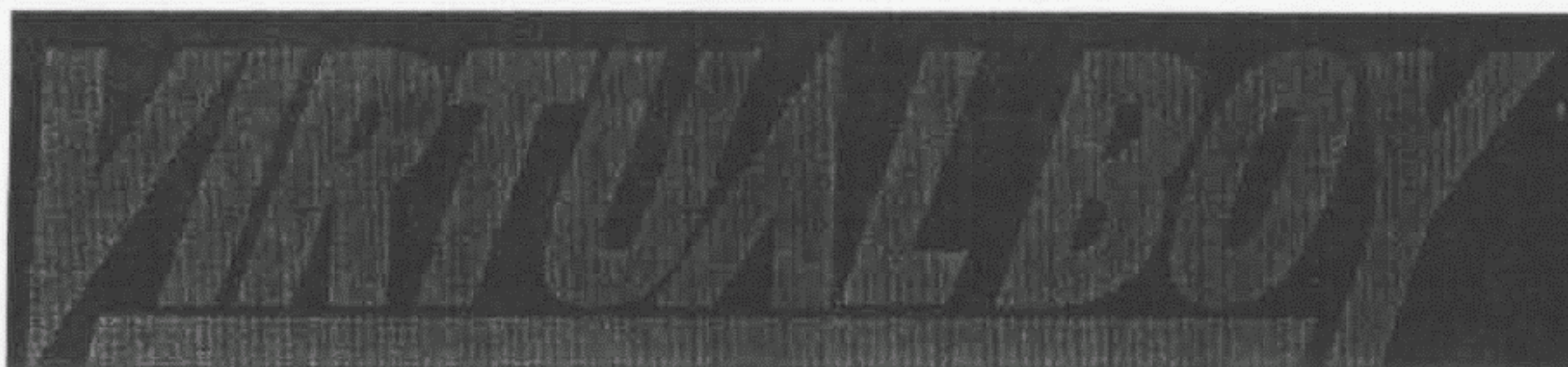
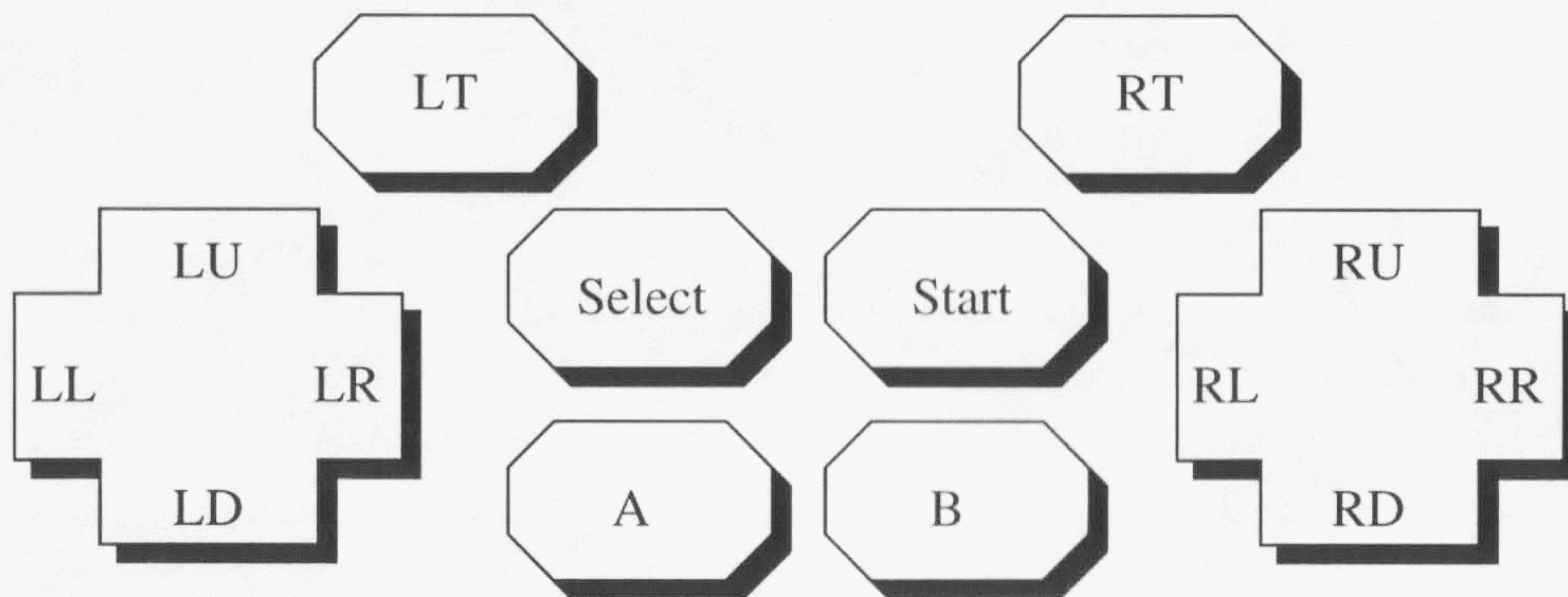


Serial Port can also be configured to generate an IRQ

Serial Port Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD	RL	SEL	STA	LU	LD	LL	LR	RR	RU	LT	RT	B	A	SGN	PWR

■ Serial Data Register (SD)



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Serial Port Control Register

7	6	5	4	3	2	1	8
K-Int-Inh	RFU	Para / Si	Soft-Ck	RFU	HW-SI	SI-Stat	S-ABT/Dis

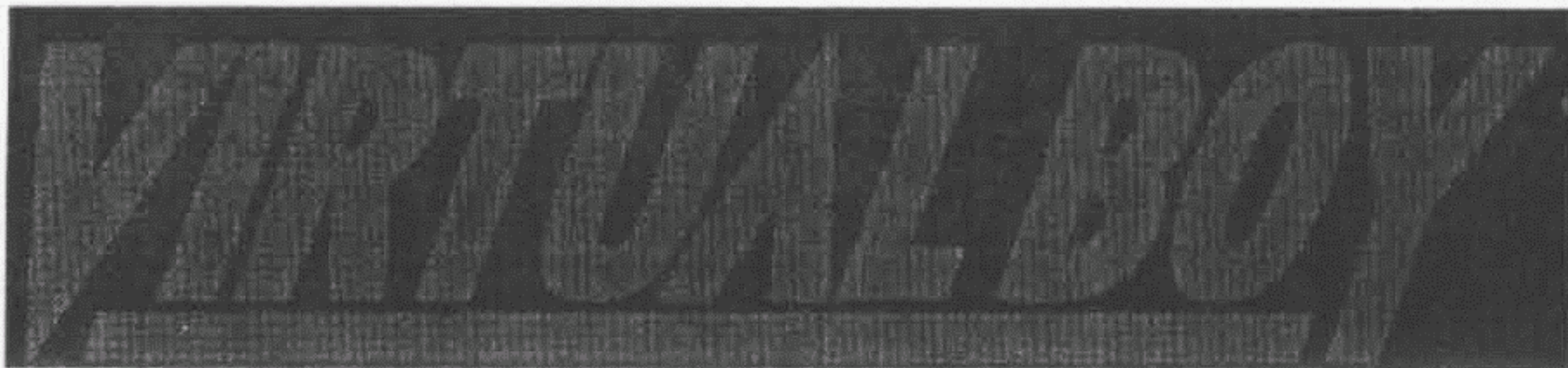
■ Serial Control Register (SCR)

- Provide access and control of the serial controller port



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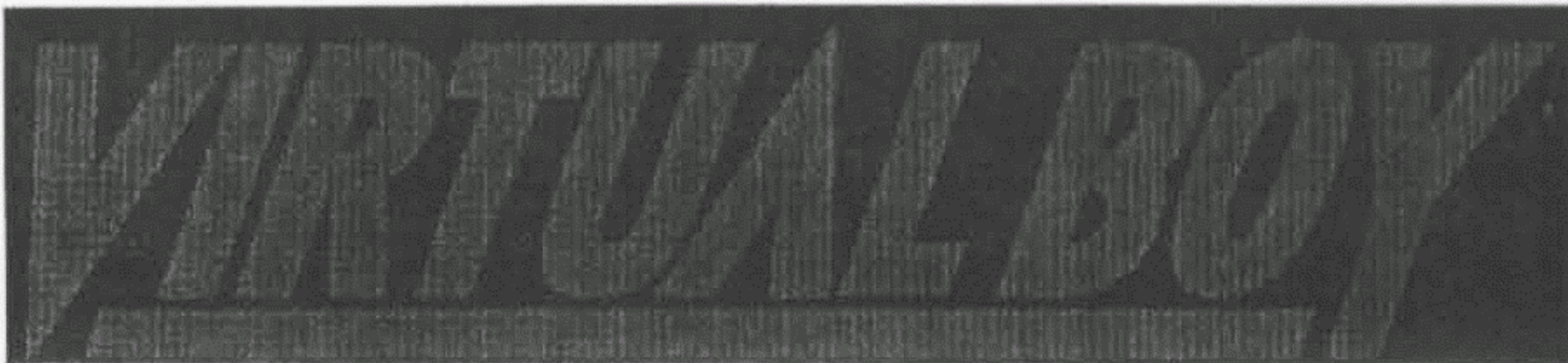
Communications Port



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Communications Port

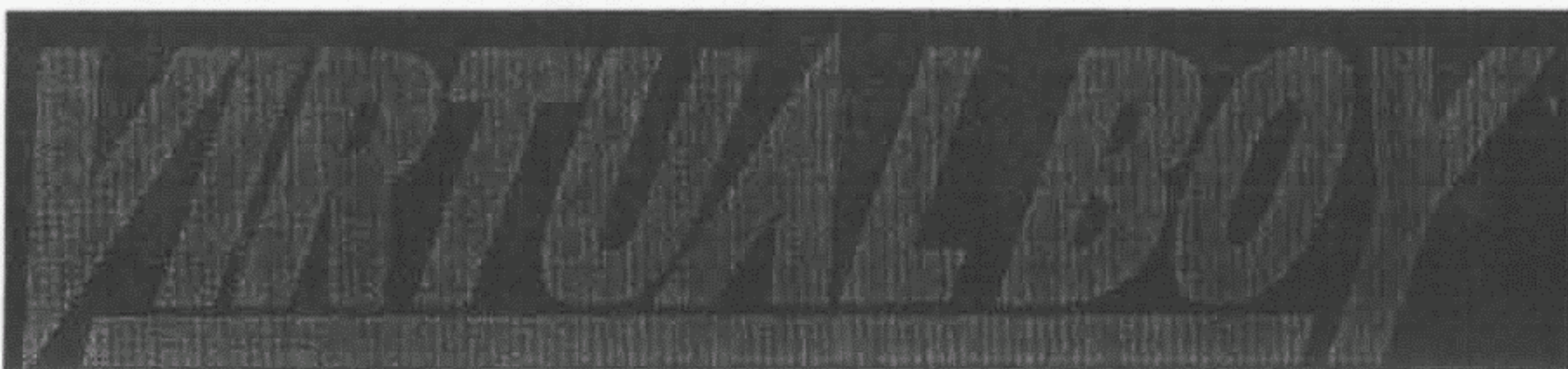
- Synchronous master / slave configuration
 - ◆ Master provides the clock
- 50 KHz clock rate
- Hardware hand shaking (C-STAT flag) with IRQ (if enabled)
- 8 bit Received / Transmitted Data Registers.



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Transmitter Protocol

- Select internal or external communication clock.
- Set the transmission data in CDTR register
- Set C-Start flag to '1'
- The C-Stat flag is set to '0' at the end of transmission
 - ◆ IRQ occurs if enabled



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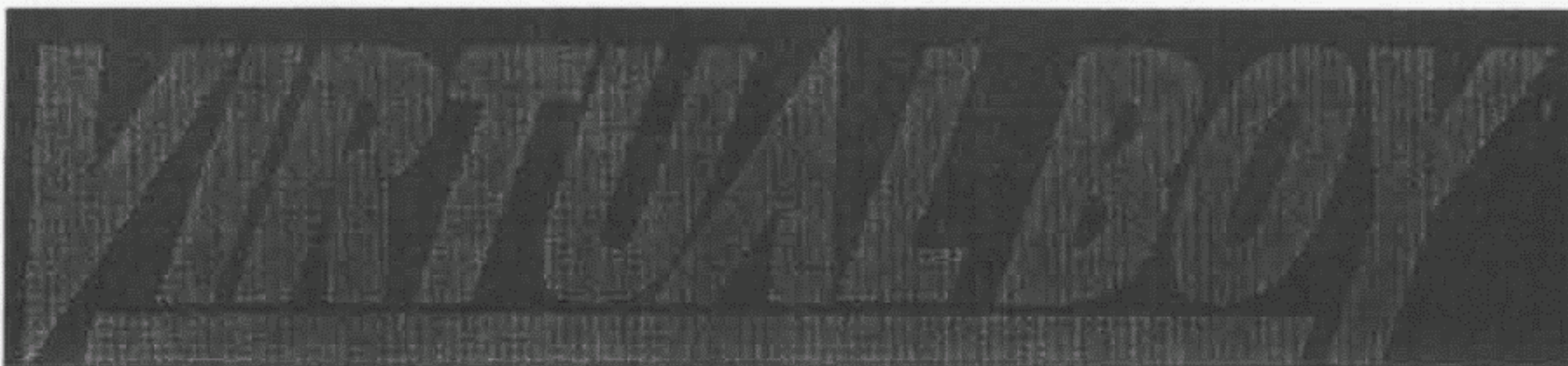
Receiver Protocol

- Set the C-Start flag to '1'
- Check if the C-Stat flag is 1
- The C-Stat flag is set to '0' at the end of data transfer.
 - ♦ IRQ occurs if enabled
- Read the received data from the CDRR register.



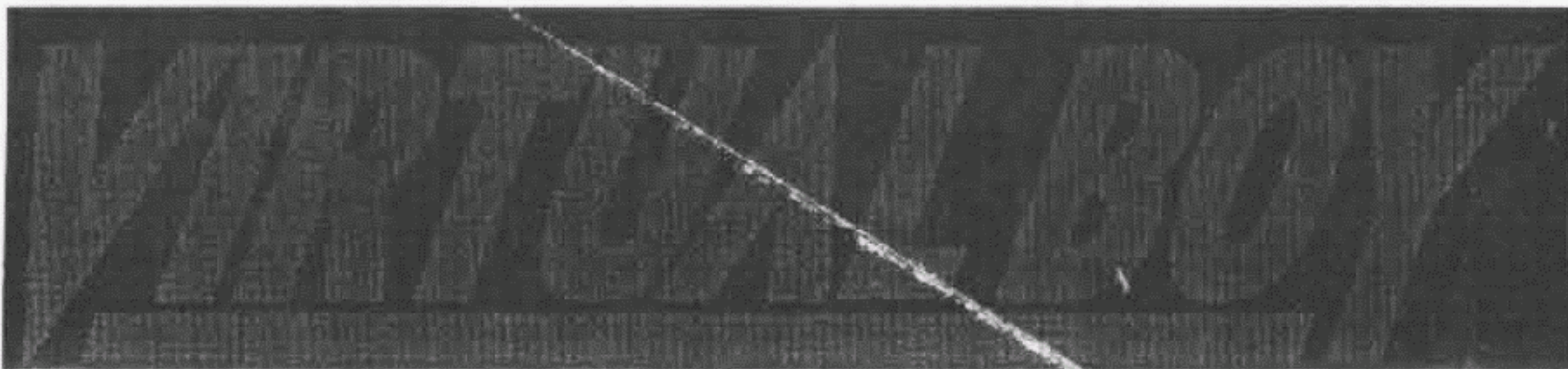
Communications Port Applications

- Multi-Player Games
 - ◆ More then two players?
- High Speed Devices (modems, etc...)



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Thank You For Attending



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